Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2018

Subject Name: CMOS VLSI Design

Subject Code: 5TE01CVD1 Branch: M.Tech (VESD)

Semester: 1 Date: 19/03/2018 Time: 02:30 To 05:30 Marks: 70

Instructions:

(1) Use of Programmable calculator and any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

SECTION – I

Q-1 **Define the following terms** **(07)**

a. Noise Margin
b. Transistor sizing.
c. Threshold Voltage.
d. Transmission Gate
e. Body effect
f. Static Power Consumption.
g. Power Delay Product.

Q-2 **Attempt all questions** **(14)**

(a) Explain the minimization of RC effect in CMOS inverter chain.
(b) Explain the characteristic and operation of NMOS Enhancement transistor.

OR

Q-2 **Attempt all questions** **(14)**

(a) Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.
(b) Explain with neat diagrams the Multiplexer and latches using Transmission Gate.

Q-3 **Attempt all questions** **(14)**

(a) Derive the equation of fall time for CMOS inverter.
(b) Design a circuit and layout diagram for two input CMOS NAND and NOR gate.

OR

Q-3 **Attempt all questions** **(14)**

(a) Derive the capacitances of three regions of operation of MOS device.
(b) Explain the fringing effects in MOS device.

SECTION – II

Q-4 **Define the following terms** **(07)**

a. Tri-state logic
b. Bi-directional Pads
c. Dynamic MOS RAM Cell
d. Routing capacitance of MOS
e. Synchronous Counter
f. Latch
g. Ripple Carry

Q-5 **Attempt all questions** **(14)**

(a) Explain Pseudo 2-phase memory structures.
(b) Write note on Clocked CMOS logic.

OR

Q-5 **Attempt all questions** **(14)**

(a) Draw and explain Pseudo nMOS logic in detail.
(b) Explain Pseudo 4-phase clocking

Q-6 **Attempt all questions** **(14)**

(a) Explain with diagram the IDDQ testing.
(b) Explain the design of Dynamic Combinational Adder.

OR

Q-6 **Attempt all Questions** **(14)**

(a) Explain the design of Booth multiplier circuit.
(b) Explain the parallel multiplier based on partial product generation.